REMARKS

This amendment is a full and timely response to the Office Action mailed June 1, 2007. Reexamination and reconsideration are respectfully requested.

Applicant appreciates Examiner's acknowledgement of the receipt of Priority Documents and consideration of the references cited in the July 6, 2005 Information Disclosure Statement.

Drawings

Figure 6, which is described in Applicant's specification as depicting conventional arts, has been amended to include the legend "Prior Art," as requested in the June 1 Action.

Abstract

The Abstract has been amended to avoid usage of the form and legal phraseology often used in patent claims, as requested in the June 1 Action.

Claims

Idiomatic corrections suggested by the Examiner in the June 1 action have been adopted as appropriate.

Claims 1-7 were rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement. This rejection is respectfully traversed.

The June 1 Action apparently finds that the second timing detecting means recited in claims 1 and the second timing detection recited in claim 7 are not properly supported by Applicant's disclosure. Applicant's claim 1 recites

> *second timing detecting means for detecting the timing of change in the level of the output signal from said oversampling means,*

while claim 7 recites

> *generating the clock timing signal according to the timing of 2N periods of said reference clock signal, said timing being detected in . . . timing of change in the level of the signal generated by said oversampling.*

Both of these recitations are fully supported by Applicant's specification. The June 1 Action states that "the waveforms S2 and S5 generated by the second timing detecting means shown in Fig. 5 do not *change the timing* in the level of the output signal S1 from said oversampling means" (emphasis added). This may be an accurate statement; however it is not germane to what Applicant has claimed. Claim does not recite a means "for changing the timing," but rather a means "for detecting the timing of change." As can be seen in Fig. 5, the one-period edge extracting circuit **30** outputs a single pulse on S2 (i.e., detects) at every time a change occurs in signal S1 (i.e., the timing of change) (e.g., at T501, T504, and T505). Similarly, claim 7 recites "timing detected in . . . timing of change," not changing any timings. Therefore claims 1 and 7 (and, furthermore, all dependent claims) are properly enabled by the specification and Applicant respectfully requests that this rejection under 35 U.S.C. § 112, first paragraph, be withdrawn.

Claim 7 was rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. This rejection is respectfully traversed.

The June 1 Action states that the term "said timing being detected in a period of time in which the level of a signal generated by said oversampling remains unchanged, and timing of change in the level of the signal generated by said oversampling" is not understood. "The test for definiteness under 35 U.S.C. 112, second paragraph, is whether "*those skilled in the art* would understand what is claimed when the claim is read *in light of the specification.*" MPEP 2173.02 (citing *Orthokinetics, Inc. v. Safety Travel Chairs, Inc.*, 806 F.2d 1565 (Fed. Cir. 1986) (emphasis added). "Only when a claim remains *insolubly* ambiguous without a discernible meaning after *all reasonable attempts* at construction must a court declare it indefinite." *Metabolite Labs., Inc. v. Lab. Corp.*, 370 F.3d 1354 (Fed. Cir. 2004) (emphasis added).

Applicant's specification teaches a method of recovering a clock signal for accurately recovering transmitted data. According to the specification, the input signal S1 is oversampled by at least a factor of four using the reference clock signal CLK. (Applicants specification, at pages 9, 19-20). In other words, if the input signal is transmitted at a data rate of 500Mbps (500,000,000 bits per second) then the reference clock has a frequency of 2 GHz (2,000,000,000 clock cycles per second). (*Id.*, at page 9). This oversampling multiple can be even greater than four, as long as it is an even multiple (i.e., the factor must be of the form 2N, where N is an integer). (*Id.*, at pages 19-20). Under ideal circumstances, every bit transmitted in S1 would have a duration equivalent to four cycles of CLK. However, if the input data signal is includes jitter, some of the bits transmitted in S1 may have a longer duration, while others may have a shorter duration. To ensure this data is interpreted properly, Applicant's specification teaches generating a modified clock signal CLKOUT which matches the bit rate of the input signal, modified to correspond with the specific jitters. For example Fig. 5 shows a data signal S1 in which the duration of the second, third, and fifth transmitted bits are of a shorter duration (3, 2, and 3 cycles of CLK, respectively). (*Id.*, at pages 14-15). To compensate for these jitters, the corresponding cycles of CLKOUT are 3, 2, and 3 CLK-cycles long, respectively. Using this modified clock signal, the input signal S1 (shifted for improved performance reasons by 1 CLK-cycle to be signal DATA) can be accurately sampled to extract the transmitted information. (*Id.*, at pages 17-18).

To generate this modified clock (i.e., detect when a new bit is being transmitted in signal S1), Applicant's specification teaches two circuits. The first circuit (comprising two-period edge extracting circuit **40** and two-period toggle circuit **50**) detects a new bit when the input signal has remained constant for at least six CLK-cycles. (*Id.*, at pages 15-16). Two-period edge extracting circuit **40** detects a transition in S1 and generates a two-CLK-cycle pulse on S3. When this two-CLK-cyle pulse ends, two-period toggle circuit **50** begins to generate a 4-CLK-cycle square wave on S4. Every new pulse generated by the two-period edge extracting circuit **40** on S3 will reset the two-period toggle circuit **50** and suppress the square wave on S4. Thus, S4 will send a 2-CLK-cycle pulse (i.e., detect the timing of a new transmitted bit) every four CLK-cycles if and only if S1 remains unchanged for a sufficient period of time.

The second circuit (comprising one-period edge extracting circuit **30** and two-period shift circuit **60**) detects a new bit whenever the input signal changes. (*Id.*, at pages 16-17). One-period edge extracting circuit **30** detects a transition in S1 and generates a one-CLK-cycle pulse on S2. To align this clock pulse with the output of the first circuit, two-period shift circuit **60** delays the pulse by two periods on output S5. Thus, S5 will send a 1-CLK-cycle pulse (i.e., detect the timing of a new transmitted bit) at timings corresponding to the timings of every change in S1.

The combined output of these two circuits is logically summed to generate the modified clock signal CLKOUT. (*Id.*, at page 17). Essentially, the second circuit detects the clock timings associated with every bit that is different from its predecessor in S1, while the first circuit detects the clock timings associated with every bit that is identical to its predecessor in S1. By combining these two sets of detected clock timings, a complete, accurate clock timing is generated.

In light of these teachings in Applicant's specification, regarding claim 7, one skilled in the art would reasonably understand said timing to refer to the timings of the generated clock signal, which are detected both when S1 (i.e., a signal generated by said oversampling) remains unchanged for a period of time (e.g., in one preferred embodiment, at least six cycles of CLK, followed by each additional four cycles of CLK during which S1 remains unchanged), and at all instances of change (i.e., cumulatively, the timing of change) in S1 (i.e., the signal generated by said oversampling). Furthermore, this element of claim 7 contains no contradiction; as taught in Applicant's specification, the timing for the clock signal CLKOUT is created by combining the detected timings of the first and second circuit.

Therefore, Applicant submits that claim 7 meets the legal requirements of 35 U.S.C. § 112, second paragraph, as one having skill in the art could reasonably interpret the metes and bounds of the claim, especially when read in light of Applicant's specification. Accordingly, Applicant respectfully requests that this rejection under 35 U.S.C. § 112, second paragraph, be withdrawn. Applicant of course welcomes any specific suggestions Examiner might propose

with regards to remaining § 112 issues concerning claim 7 which would not affect the scope of claimed subject matter.

In view of the above amendment, applicant believes the pending application is in condition for allowance.

Applicant believes no fee is due with this response. However, if a fee is due, please charge our Deposit Account No. 18-0013, under Order No. SON-2937 from which the undersigned is authorized to draw.

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Respectfully submitted,

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Attachments

REPLACEMENT SHEET